Amendment to the Claims:

The listing of claims will replace all prior versions, and listings of claims in the application:

Listing of Claims:

1-16. Cancelled (Without disclaimer or prejudice).

17. (New) A method for identifying a data packet in a data stream in which

a d.c. voltage quota for a demodulated digital input signal is calculated in that the input signal is scanned in order to generate a sequence of scanned values corresponding to the input signal and from a selected number of scanned values the d.c. voltage quota of the input signal is calculated;

a k-bit word is allocated to the input signal in that for each symbol of the input signal corresponding to a bit, a bit value is determined as a function of the d.c. voltage quota;

the k-bit word corresponding to the input signal is compared with an expected k-bit synchronization word in order to determine a correlation value; and

a packet identification signal is generated if the correlation value is greater than a correlation threshold value; and wherein

the d.c. voltage quota of the input signal is calculated again after each scan of the input signal at least until the correlation value determined by comparison of the k-bit word corresponding to the input signal with an expected k-bit synchronization word is greater than the correlation threshold value.

18. (New) The method according to Claim 17, wherein after a packet identification signal has been generated the corresponding correlation value is stored and scanning of the input signal calculation of the d.c. voltage quota and comparison of the k-bit word corresponding to the input signal with an expected k-bit synchronization word to determine the correlation value is still continued for a

predeterminable period of time and a new packet identification signal is generated if a newly determined correlation value is greater than the correlation threshold value and greater than the previously determined stored correlation value

19. (New) The method according to claim 18, wherein to determine the k-bit word corresponding to the input signal, the input signal is scanned in order to generate a sequence of scanned values corresponding to the input signal and a bit value is allocated to each scanned value of a selected multiplicity of scanned values as a function of the d.c. voltage quota of the input signal.

20. (New) The method according to claim 19, wherein the input signal is scanned at a frequency which is chosen in such a way that an the over-scanning rate is at least equal to two, that therefore at least two scanned values are determined for each symbol and to form the k-bit word corresponding to the input signal in each case only one scanned value per symbol is selected.

21. (New) The method according to Claim 18, wherein the multiplicity of scanned values for forming the k-bit word corresponding to the input signal is selected from the sequence of scanned values in such a way that the selected scanned values within the sequence in each case are substantially the same distance apart.

22. (New) The method according to claim 21, wherein the number of scanned values for calculating the d.c. voltage quota of the input signal is chosen in such a way that the scanned values correspond to areas in the expected k-bit synchronization word which substantially have the same number of bits with the value 0 and bits with the value 1 and the d.c. voltage quota is calculated as an average value of the scanned values.

23. (New) The method according to Claim 22, wherein the number of scanned values for calculating the d.c. voltage quota consists of at least one group of scanned values in direct succession to one another, which correspond to successive symbols.

24. (New) The method according to Claim 22, wherein the number of scanned values for calculating the d.c. voltage quota consists of two groups of scanned values, which are separated from one another by scanned values.

25. (New) A device for identifying data packets in a data receiving stream with a delay line which has a number of storage places, in which scanned values of a demodulated digital input signal are stored in series, a d.c. voltage quota determining circuit, which is connected to the delay line in order to calculate a d.c. voltage quota of the input signal as an average value of a selected number of scanned values comprising:

a decoding circuit connected to the delay line and the d.c. voltage quota determining circuit which compares a multiplicity of scanned values with the d.c. voltage quota in order to allocate a bit value to each scanned value and in this way to form a k-bit word corresponding to the input signal;

a comparison and correlation calculating circuit which compares the k-bit word corresponding to the input signal with an expected k-bit synchronization word and calculates a correlation value for the k-bit word corresponding to the input signal; and

a correlation value comparison circuit which compares the correlation value supplied by the comparison and correlation calculating circuit with a correlation threshold value in order to supply a packet identification signal if the correlation value is greater than or equal to the correlation threshold value; and wherein

the decoding circuit comprises a multiplicity k of comparison circuits, to which in each case is applied the d.c. voltage quota and each of which is connected to one of the storage places of the delay line in order to compare the respective scanned

value with the d.c. voltage quota and to determine a bit value, so the k-bit word corresponding to the input signal is applied to outputs of the decoding circuit.

26. (New) The device according to Claim 25, wherein the number of storage places of the delay line corresponds to the number k of bits in the k-bit synchronization word multiplied by the over-scanning rate, in other words with the number of scanned values per symbol.

27. (New) A device for identifying data packets in a data receiving stream with a delay line which has a number of storage places, in which scanned values of a demodulated digital input signal are stored in series, and a d.c. voltage quota determining circuit, which is connected to the delay line in order to calculate a d.c. voltage quota of the input signal as an average value of a selected number of scanned values comprising:

a decoding circuit connected to the delay line and the d.c. voltage quota determining circuit which compares a multiplicity of scanned values with the d.c. voltage quota in order to allocate a bit value to each scanned value and to form a k-bit word corresponding to the input signal;

a comparison and correlation calculating circuit which compares the k-bit word corresponding to the input signal with an expected k-bit synchronization word and calculates a correlation value for the k-bit word corresponding to the input signal; and

a correlation value comparison circuit which compares the correlation value supplied by the comparison and correlation calculating circuit with a correlation threshold value in order to supply a packet identification signal if the correlation value is greater than or equal to the correlation threshold value; and wherein

the d.c. voltage quota determining circuit has at least one addition circuit and one division circuit connected to the output of the addition circuit via a holding element;

one input of the addition circuit is connected to a first storage place of the delay line and another input is connected to a second storage place of the delay

line, which is separated from the first storage place by a multiplicity of storage places; and

the input, which is connected to the second storage place, is negated and the output of the addition circuit is fed back to a third input via the holding element, so that with each addition the result of the preceding addition is added on and wherein a sum supplied by the holding circuit is divided in the division circuit by a value corresponding to the distance between the storage places in order to calculate the d.c. voltage quota.

28. (New) The device according to Claim 27, wherein two addition circuits connected to storage places of the delay line are provided, output signals of which are supplied to the division circuit via a further addition circuit.

29. (New) The device according to Claim 28, wherein the comparison and correlation calculating circuit connected to the decoding circuit and a register storing the expected k-bit synchronization word, besides a multiplicity k of comparison circuits for comparing the k-bit word supplied by the decoding circuit and corresponding to the input signal with the k-bit synchronization word, has a correlation element which adds a one for each coinciding bit pair in order to calculate the correlation value.

30. (New) The method according to Claim 17, wherein after a packet identification signal has been generated the corresponding correlation value is stored and scanning of the input signal, calculation of the d.c. voltage quota and comparison of the k-bit word corresponding to the input signal with an expected k-bit synchronization word to determine the correlation value is still continued for a predeterminable period of time and a new packet identification signal is generated if a newly determined correlation value is greater than the correlation threshold value and greater than the previously determined stored correlation value.

31. (New) The method according to Claim 23, wherein the number of scanned values for calculating the d.c. voltage quota consists of two groups of

scanned values, which are separated from one another by a multiplicity of scanned values.

32. (New) The device according to Claim 26, wherein the decoding circuit comprises a multiplicity k of comparison circuits, to which in each case is applied the d.c. voltage quota and each of which is connected to one of the storage places of the delay line in order to compare the respective scanned value with the d.c. voltage quota and to determine a bit value, so a k-bit word corresponding to the input signal is applied to outputs of the decoding circuit.

33. (New) The device according to Claim 26, wherein the d.c. voltage quota determining circuit has at least one addition circuit and one division circuit connected to the output of the addition circuit via a holding element , wherein one input of the addition circuit is connected to a first storage place of the delay line and another input is connected to a second storage place of the delay line which is separated from the first storage place by a multiplicity of storage places; and

the input which is connected to the second storage place is negated and the output of the addition circuit is fed back to a third input via the holding element, so that with each addition the result of the preceding addition is added on and wherein the sum supplied by the holding circuit is divided in the division circuit by a value corresponding to the distance between the storage places in order to calculate the d.c. voltage quota.

34. (New) The device according to Claim 25, wherein the d.c. voltage quota determining circuit has at least one addition circuit and one division circuit connected to the output of the addition circuit via a holding element, wherein one input of the addition circuit is connected to a first storage place of the delay line and another input is connected to a second storage place of the delay line which is separated from the first storage place by a multiplicity of storage places; and

the input which is connected to the second storage place is negated and the output of the addition circuit is fed back to a third input via the holding element, so that with each addition the result of the preceding addition is added on and wherein

a sum supplied by the holding circuit is divided in the division circuit by a value corresponding to the distance between the storage places in order to calculate the d.c. voltage quota.